AMENDMENTS TO THE CLAIMS

Upon entry of the present amendment, the status of the claims will be as shown below. This listing of claims replaces all previous versions and listings of the claims in the present application.

Listing of Claims:

1 (Currently Amended). A plasma display driven by a subfield system, the plasma display comprising:

a plurality of discharge cells;

a clock signal generator that generates a clock signal;

a serial data generator that generates serial data according to an image to be displayed;

a test signal generator that generates a test signal;

a data driver that selectively applies a drive pulse to said plurality of discharge cells based on the serial data generated by said serial data generator in synchronization with said clock signal in a write period for selecting a discharge cell to be lighted;

a latch failure detector that includes a latcher that latches the test signal generated by said test signal generator to detect a presence/absence of a latch failure in said data driver based on an output signal from said latcher in ~~a period other than said write period; and~~ an adjustment period including a sustain period during which light emission of the discharge cell selected in said write period is sustained;

a phase adjuster that, when the latch failure is detected by said latch failure detector, adjusts a phase of the clock signal provided ~~from~~ by said clock signal generator to said data driver, based on the phase of the clock signal in which the latch failure is detected; and

a first storage device that stores the phase of the clock signal adjusted by said phase adjuster as an optimal phase,

wherein said phase adjuster varies the phase of said clock signal to detect a phase range within which a latch failure does not occur, and stores, in said first storage device, a phase in a center of said detected phase range as said optimal phase during said adjustment period, and adjusts the phase of said clock signal to said optimal phase stored in said first storage device in the write period after said optimal phase is stored by said first storage device.

2 (Currently Amended). The plasma display according to claim 1,

wherein said data driver includes a plurality of data drivers;

said latch failure detector includes a plurality of latch failure detectors that detect the presence/absence of the latch failure by respective data drivers based on the test signal ~~outputted~~ output from said test signal generator; and

when the latch failure is detected in at least one of said plurality of latch failure detectors, said phase adjuster adjusts the phase of the clock signal provided to said plurality of data drivers from said clock signal generator.

3 (Currently Amended). The plasma display according to claim 2,

wherein said plurality of latch failure detectors each have an open drain output; and

said phase adjuster receives the open drain outputs of said plurality of latch failure detectors via a wired-OR connection.

4 (Currently Amended). The plasma display according to claim 1, wherein said test signal is an alternating pulse signal that is inverted every period of said clock signal.

5 (Currently Amended). The plasma display according to claim 1, wherein said phase adjuster adjusts the phase of the clock signal at predetermined intervals.

6 (Currently Amended). The plasma display according to claim 1, wherein said phase adjuster adjusts the phase of the clock signal at intervals of a plurality of fields.

7 (Currently Amended). The plasma display according to claim 1, wherein said phase adjustment includes a plurality of phase adjustment periods; and

said phase adjuster continues, when the adjustment of said phase of the clock signal has not finished in one adjustment period, the phase adjustment of said phase of the clock signal from the beginning of the next adjustment period.

8 (Currently Amended). The plasma display according to claim 4, wherein said latch failure detector generates a latch failure detection signal indicating the presence/absence of the latch failure, based on an exclusive logical sum of a first test signal obtained by delaying said test signal by one period of said clock signal and a second test signal obtained by delaying said test signal by two periods of said clock signal.

9 (Currently Amended). The plasma display according to claim 8, wherein said latch failure detector generates a plurality of latch failure detection signals obtained by sequentially delaying said latch failure detection signal by a predetermined delay amount to generate a logical product of said plurality of latch failure detection signals.

10 (Currently Amended). The plasma display according to claim 1, wherein said latch failure detector includes a holder that holds a detection result of the latch failure until a reset signal is inputted.

11 (Currently Amended). The plasma display according to claim 10, wherein said latch failure detector further includes a reset signal generator that generates said reset signal based on the detection result of the latch failure.

12 (canceled).

13 (Currently Amended). The plasma display according to claim 1,

wherein said phase adjuster includes:

a ring buffer including a plurality of delay elements that sequentially delay said clock signal by a predetermined delay amount; and

a selector that selectively outputs a plurality of clock signals ~~outputted~~ output from said plurality of delay elements of said ring buffer.

14 (currently amended). The plasma display according to claim 1,

wherein said phase adjuster includes:

a plurality of delays each having a different number of delay amounts; and

a connector that selects one or more of said plurality of delays so as to constitute a series-connector by the selected one or more of said plurality of delays and provides said clock signal to said series-connector.

15 (canceled).

16 (Currently Amended). The plasma display according to claim 1, wherein the phase adjuster is operable to detect that the phase of the adjusted clock signal is an optimal phase and

to finish the adjustment of the phase of said clock signal when it is detected that the phase of the clock signal is the optimal phase.

17 (canceled).

18 (Currently Amended). The plasma display according to claim ~~17~~ 1, wherein said phase adjuster adjusts the phase of said clock signal to a phase stored in advance in said first storage device when the adjustment of said phase of the clock signal has not finished in said adjustment period.

19 (Currently Amended). The plasma display according to claim ~~17~~ 1, wherein said phase adjuster ~~varies the phase of said clock signal to detect a range of phases where no latch failure occurs and when the detected range is larger than a predetermined threshold~~, stores, in said first storage device, [[a]] the phase in [[a]] the center of said detected phase range ~~of phases~~ as said optimal phase when the detected range is larger than a predetermined threshold.

20 (Currently Amended). The plasma display according to claim ~~17~~ 1, wherein said phase adjuster adjusts a relative phase of the clock signal with respect to said serial data so that said adjusted phase of the clock signal is ~~outputted~~ output to the data driver just as a phase of a start portion of said serial data is ~~outputted~~ output to said data driver.

21 (Currently Amended). The plasma display according to claim 20, wherein, said phase adjuster adjusts the phase of said serial data so that the phase of ~~the~~ a start portion of the serial data ~~outputted~~ output to said data driver and a phase of a start portion of the clock signal

~~outputted~~ output to said data driver substantially coincide with each other when it is detected that the phase of said clock signal is the optimal phase.

22 (Currently Amended). The plasma display according to claim 21, further comprising a second storage device that stores the phase of said serial data adjusted by said phase adjuster as an optimal phase,

wherein said phase adjuster adjusts the phase of said serial data to said optimal phase stored in said second storage device in the write period after said optimal phase is detected by said second storage device.

23 (Currently Amended). The plasma display according to claim 22, wherein said phase adjuster adjusts the phase of said clock signal to the optimal phase stored in said first storage device a last time and adjusts the phase of said serial data to the optimal phase stored in said second storage device a last time when the optimal phase of said clock signal or the optimal phase of said serial data is not detected.

24-26 (canceled).